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In this paper, we describe some of the attributes of the SCISM organization, a multiphase outcome of five years of research at the IBM Glendale Laboratory, in Endicott, New York. The organization embodies a number ...

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2 [Implications of structured programming for machine architecture](#)

Andrew S. Tanenbaum

March 1978 **Communications of the ACM**, Volume 21 Issue 3**Publisher:** ACM [Request Permissions](#)Full text available: [Pdf](#) (1.08 MB)[Additional Information:](#) full citation, abstract, references,**Bibliometrics:** Downloads (6 Weeks): 7, Downloads (12 Months): 31, Downloads (Overall): 30

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Based on an empirical study of more than 10,000 lines of program text written in a C-like architecture specifically designed for structured programs is proposed. Since assignment statements together account ...

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Keywords: computer architecture, computer organization, instruction set design, microprocessor characteristics

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3 [Three extensions to register integration](#)

Vlad Petric, Anne Bracy, Amir Roth

November 2002 **MI CRO 35**: Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**Publisher:** IEEE Computer Society PressFull text available: [Publisher Site](#), [Pdf](#) (1.37 MB) [Additional Information:](#) full citation, abstract, references,**Bibliometrics:** Downloads (6 Weeks): 3, Downloads (12 Months): 9, Downloads (Overall): 147

Register integration (or just integration) is a register renaming discipline that implements physical register sharing. Initially developed to perform squash reuse, the integration reuse scenarios. Here, ...

4 [A simple graph-based intermediate representation](#)

Cliff Click, Michael Paleczny

March 1995 **Papers from the 1995 ACM SIGPLAN workshop on Intermediate representations****Publisher:** ACMFull text available: [Pdf](#) (157.59 KB)[Additional Information:](#) full citation, abstract, references,**Bibliometrics:** Downloads (6 Weeks): 17, Downloads (12 Months): 79, Downloads (Overall): 467

We present a graph-based intermediate representation (IR) with simple semantics and a simple implementation. The IR uses a directed graph with labeled vertices and ordered input/output edges. Vertices are labeled with opcodes, ...

Also published in:

March 1995 SIGPLAN Notices Volume 30 Issue 3

5 The design of a space efficient compiler

 Michael K. Donegan
August 1978 **SLGM**

August 1978 **SIGMINI '78**: Proceedings of the first SIGMINI symposium on Small systems

Publisher: ACM Request PermissionsFull text available: Pdf (449.01 KB)

Additional Information: full citation, abstract, references.


Bibliometrics: Downloads (6 Weeks): 5. Downloads (12 Months): 11. Downloads (Overall): 82

Writing a compiler for a small machine with minimal software support can be quite difficult. The usual techniques for writing compilers are usually inadequate. In addition, the usual techniques for writing compilers produce programs which are ...

Also published in:

August 1978 SIGMINI Newsletter Volume 4 Issue 4

6 MicroTAL - a machine-dependent, high-level microprogramming language

 Joel F. Bartlett
December 1981

December 1981 **MICRO 14:** Proceedings of the 14th annual workshop on Microprogramm

Publisher: ACM

Full text available: Pdf (413.24 KB)

Additional Information: full citation, abstract, references.

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 7, Downloads (Overall): 70.

The design and implementation of a high-level microprogramming language is described in this paper. The language is based on an existing systems programming language, TAL, which allows algorithms to be written in a high-level microprogramming language. The procedure may ...

Also published in:

December 1981 SIGMICRO Newsletter Volume 12 Issue 4

7 Measuring VAX 8800 performance with a histogram hardware monitor

 D. W. Clark, P. J. Bannon, J. B. Keller
June 1988 **ISCA '88: Proceedings**

June 1988 **ISCA '88:** Proceedings of the 15th Annual International Symposium on Co

Publisher: ACM

Full text available: Pdf (1.04 MB)

Additional Information: full citation, abstract, references.

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 23, Downloads (Overall): 14

This paper reports the results of a study of VAX 8800 processor performance using a histograms of the processor's micro-PC and memory bus status. The monitor keeps a executed at each micro-PC ...

Also published in:

May 1988 SIGARCH Computer Architecture News Volume 16 Issue 2

8 On the introduction of reconfigurable hardware into computer architecture education

 Ross Brennan, Michael Manzke

June 2003 **WCAE '03**: Proceedings of the 2003 workshop on Computer architecture and
with the 30th International Symposium on Computer Architecture

Publisher: ACM

Full text available:  Pdf (233.83 KB)

Additional Information: full citation, abstract, references

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 23, Downloads (Overall): 42

The introduction of reconfigurable logic devices as teaching-aids, into undergraduate enables the students to conduct experiments they could otherwise not perform. Further instructors the freedom to choose ...

- 9 [Cycle-accurate energy consumption measurement and analysis: case study of A Naehyuck Chang, Kwanho Kim, Hyung Gyu Lee](#)
August 2000 **ISLPED '00: Proceedings of the 2000 international symposium on Low pow**

Publisher: ACM [Request Permissions](#)

Full text available: [Pdf](#) (129.03 KB)

Additional Information: [full citation](#), [abstract](#), [references](#).

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 39, Downloads (Overall): 52

We introduce an energy consumption analysis of complex digital systems through a processor by using a new energy measurement technique. We developed a cycle-accurate measurement system based on charge transfer ...

- 10 [Concept and synthesis of an operating system nucleus implemented in computer Jan Kazimierzczak](#)
February 1987 **CSC '87: Proceedings of the 15th annual conference on Computer Science**

Publisher: ACM [Request Permissions](#)

Full text available: [Pdf](#) (1.28 MB)

Additional Information: [full citation](#), [abstract](#), [references](#).

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 6, Downloads (Overall): 99,

In this paper a concept of an operating system nucleus is introduced and its synthesis concept the operating system nucleus should be realized as hardware that generates parts of the programs ...

- 11 [A microcoded RISC D. K. DuBose, D. K. Fotakis, D. Tabak](#)
December 1986 **MICRO 19: Proceedings of the 19th annual workshop on Microprogram**

Publisher: ACM

Full text available: [Pdf](#) (409.75 KB)

Additional Information: [full citation](#), [abstract](#), [references](#).

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 7, Downloads (Overall): 115

A new, microcoded, RISC-type system is proposed and presented. The microcode is a Nanomemory in the CPU. The 8-bit opcode of each instruction is a direct address to the Nanomemory 64-bit word (horizontal microcode) ...

Also published in:

December 1986 **SIGMICRO Newsletter** Volume 17 Issue 4

- 12 [Low-cost branch folding for embedded applications with small tight loops Lea Hwang Lee, Jeff Scott, Bill Moyer, John Arends](#)
November 1999 **MICRO 32: Proceedings of the 32nd annual ACM/IEEE international sym**

Publisher: IEEE Computer Society

Full text available: [Publisher Site](#), [Pdf](#) (953.19 KB) **Additional Information:** [full citation](#), [abstract](#), [refer](#)

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 21, Downloads (Overall): 37

Many portable and embedded applications are characterized by spending a large fraction of program loops. To improve performance, many embedded systems use special instruction executions. These special ...

- 13 [A comparison of the code space and execution time required for FORTRAN assembly computer architectures Richard A. Belgard, Victor B. Schneider](#)

December 1978 **MICRO 11**: Proceedings of the 11th annual workshop on Microprogram

Publisher: ACM

Full text available:  Pdf (470.08 KB)

Additional Information: [full citation](#), [abstract](#), [references](#).

Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 11, Downloads (Overall): 70

A method is presented for deriving lower and upper bounds for memory space and execution time for FORTRAN assignment statements. Formulas, in terms of variable references, are presented for six hypothetical computer architectures, ...

Also published in:

December 1978 **SIGMICRO Newsletter** Volume 9 Issue 4

14 [A microcoded RISC](#)

 D. K. DuBose, D. K. Fotakis, D. Tabak

June 1986 **SIGARCH Computer Architecture News**, Volume 14 Issue 3

Publisher: ACM

Full text available:  Pdf (363.51 KB)

Additional Information: [full citation](#), [abstract](#), [cited by](#), [in](#)

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 8, Downloads (Overall): 76,


A new, microcoded, RISC-type system is proposed and presented. The microcode is stored in Nanomemory in the CPU. The 8-bit opcode of each instruction is a direct address to the Nanomemory 64-bit word (horizontal microcode) ...

15 [Derive: a tool that automatically reverse-engineers instruction encodings](#)

 Dawson R. Engler, Wilson C. Hsieh

January 2000 **DYNAMO '00**: Proceedings of the ACM SIGPLAN workshop on Dynamic analysis and optimization

Publisher: ACM

Full text available:  Pdf (1.07 MB)

Additional Information: [full citation](#), [abstract](#), [references](#).


Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 26, Downloads (Overall): 47

Many binary tools, such as disassemblers, dynamic code generation systems, and emulators, do not understand how machine instructions are encoded. Unfortunately, specifying such encodings is error-prone. Users must typically ...

Also published in:

July 2000 **SIGPLAN Notices** Volume 35 Issue 7

16 [Generation of fast interpreters for Huffman compressed bytecode](#)

 Mario Latendresse, Marc Feeley

June 2003 **IVME '03**: Proceedings of the 2003 workshop on Interpreters, virtual machines, and embedded systems

Publisher: ACM 





Full text available:  Pdf (323.22 KB)

Additional Information: [full citation](#), [abstract](#), [references](#).

Bibliometrics: Downloads (6 Weeks): 12, Downloads (12 Months): 32, Downloads (Overall): 47

Embedded systems often have severe memory constraints requiring careful encoding of instructions. Smart cards have on the order of 1K of RAM, 16K of non-volatile memory, and 24K of flash memory. An effective approach to obtain ...

Keywords: Java, canonical Huffman code, code compression, decoder

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